DELIVERABLE REPORT

NEXUS

D2.2: Full PVSK/Si cell demonstrator with sustainable design and scalable processes, PCE >33%, for active area > 0.5 cm^2 and PCE > 31%, for 100 cm^2 active area

Deliverable D2.2
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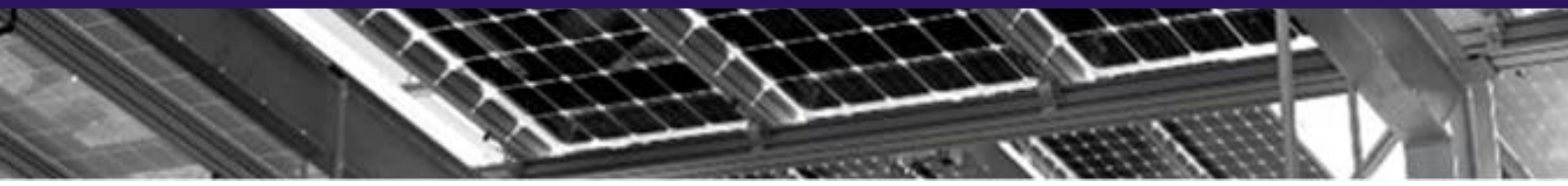

Grant Agreement n°101075330

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NEXUS aims to accelerate Europe's energy transition by developing perovskite-silicon tandem photovoltaic technology, via a new European paradigm: an eco-design approach, based on efficiency, cost, sustainability, circularity and social aspects and using abundant materials. NEXUS aims to develop stable, 2-terminal perovskite-silicon tandem solar cells and modules with high power conversion efficiencies, using sustainable, coherent and competitive European PV production, to create a viable economic pathway for the European commercialisation of this technology.

NEXUS is formed of a multi-disciplinary consortium: 13 partners from 10 countries; 6 industrial partners & 7 RTOs, covering the whole value chain of innovation from research centres to technology providers, end-users and market and policies.

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NEXUS Consortium

Organization name	Short name	Country
COMMISSARIAT A L'ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES	CEA	FR
ACCADEMIA EUROPEA DI BOLZANO	EURAC	IT
KARLSRUHER INSTITUT FUER TECHNOLOGIE	KIT	DE
RIJKSUNIVERSITEIT GRONINGEN	RUG	NL
SALD B.V	SALD	NL
UNIVERSITAT DE VALENCIA	UVEG	ES
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Table of Content

Table of Content 4
List of Tables 5
List of Figures 5
Abbreviations and acronyms list 6
1. Executive Summary 6
1.1. Description of the deliverable content and purpose 6
1.2. Relation with other activities in the project 7
2. Results 8
2.1. Introduction, tandem expected values 8
2.2. Champion tandem devices on small area 12
2.3. Large area tandem devices 14
2.3.1. Development of PST solar cells with an “intermediate” area layout 14
2.3.2. Manufacturing attempts on 100 cm^2 15
2.4. Taking eco-design one step further with Indium-free TCO layers 16
3. Discussion: NEXUS results in relation to existing literature on PST solar cells 18
4. Conclusion 20
References 22

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List of Tables

Table 1: Expected IV parameters of PST devices based on the IV parameters measured on the SJ cells composing the final tandem device. 12

List of Figures

Figure 1: Simulated external quantum efficiency (EQE) of PST solar cells with Si bottom cells based on wafers of different thicknesses: simulated structure (left), share of photons absorbed by wavelength in the perovskite absorber (dashed lines) and in the c-Si wafer (solid lines) for three wafer thicknesses (250 µm (black), 140 µm (red) and 120 µm (blue)) (right). The inset table shows the short-circuit current of each sub-cell calculated from the EQE with the AM1.5 spectrum. 9
Figure 2: Implied V_{oc} measured by Sinton technique: at 1 sun on M2 wafers after a-Si:H deposition and at 1 sun and 0.5 sun after cutting them to 3x3 cm^2 substrates (left); at 0.5 sun on 3x3 cm^2 silicon substrates after different process steps of the PVSK top cell fabrication (right), V0 corresponding to the "0.5 sun, post cutting" measurement of the left graph. For this particular substrate, a maximum V_{oc} of the bottom cell is expected to be around 0.69 V. 10
Figure 3: Best single junction top perovskite cells for the three different deposition methods. 11
Figure 4: Highest efficiency device for small area reaching 27.45% PCE by sequential method of perovskite deposition. 12
Figure 5: Tandem device with co-evaporated perovskite showing the highest efficiency for this type of deposition, PCE=27,2% (left, a). The high hysteresis may be due to contaminated SnO_2 layer. MPP tracking (center, b). Device stack (right, c). 13
Figure 6: Tandem device with perovskite deposited following the hybrid method. It reached a maximum efficiency of 27.02% (left, a). Evolution of parameters for the first 5 minutes (center, b). Device stack (right, c). 13
Figure 7: Champion device on 4.41cm2 area done with the sequential evaporation method. The PCE obtained with the champion device was 26.8%. 14
Figure 8: Process line for making 100cm^2 tandem device on M2 wafer size. 16
Figure 9: Replacement of rear ITO transparent electrode by AZO: Absorptance curves measure by spectrophotometry (a), simulated EQE of PST solar cells with either ITO (blue) or AZO (green) as rear TCO and bottom cells using either a 140 µm (darker colour) or 120 µm (lighter colour) wafer, c) Jsc values of each sub-cell for the different cases calculated from the EQE with the AM1.5 spectrum. .. 17
Figure 10: a) Standard tandem architecture using ITO as both TCO and CRJ (left, reference) and Indium free eco-design device (right) using AZO as replacement. b) JV characteristics of reference (black) and eco-friendly design (orange). In-free device achieved 18.1% PCE while in this case, the reference reached only 16.9% PCE. 18
Figure 11: Highest reported PCEs of perovskite/Si tandem solar cells for different deposition techniques plotted over area. The highest PCEs achieved within NEXUS (hybrid + vapor) are also shown. 19

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Abbreviations and acronyms list

Abbreviation	Meaning	Abbreviation	Meaning
2T	two-terminal	LCC	lifecycle costing
AZO	aluminum-doped zinc oxide	LPCVD	low pressure chemical vapor deposition
CRJ	carrier recombination junction	MPP	maximum power point
c-Si	monocrystalline silicon	NIR	near infrared
Cz	Czochralski	PCE	power conversin efficiency
EQE	external quantum efficiency	PLD	pulsed laser deposition
FF	fill factor	PST	perovskite/silicon tandem
FZ	float zone	PV	photovoltaics
GHG	greenhouse gases	SAM	self-asembled monolayer
HTL	hole transport layer	SHJ	silicon heterojuction
ITO	tin-doped indium oxide	SJ	single junction
IZO	zinc-doped indium oxide	TCO	transparent conductive oxide
J	current density	V	voltage
Jsc	short-circuit current density	Voc	open-circuit voltage
LCA	lifecycle analysis		

1. Executive Summary

1.1. Description of the deliverable content and purpose

In this deliverable, we make use of the perovskite single-junction cells developed within WP1 and integrate them with silicon bottom cells prepared at CEA using Czochralski (Cz) wafers, as described in Deliverable 2.1, to fabricate tandem devices. The initial objective is to achieve power conversion efficiencies (PCEs) of 33% on small-area devices (>0.5 cm²) and PCEs above 30% for a 100 cm² size device.

Building on the results obtained in WP1, three different methods can be distinguished for the deposition of the perovskite absorber: (a) co-sublimation of all precursors (co-evaporation method), (b) co-sublimation of the inorganic precursors followed by the addition of organic precursors in a benign solvent (hybrid method), and (c) sublimation of the inorganic precursors followed by the sublimation of the organic precursors (sequential evaporation method).

The highest efficiencies were obtained with the sequential evaporation method, reaching 27.45% for 1 cm² and 26.8% for 4.41 cm² devices. The co-evaporation and hybrid methods achieved 27.2% and 27.0% PCEs, respectively, on 1 cm² devices. These results — particularly those using fully vacuum-processed perovskites on thin industrial Cz silicon—remain noteworthy and nearly unique in current literature as they are still among the highest reported for vapor-based perovskite-Si tandem solar cells. Devices with a reduced indium content, using an In-free rear transparent electrode based on aluminum-doped zinc oxide (AZO) achieved a slightly lower PCE of 24.6%. Finally, a demonstrator, using only indium-free transparent conductive oxide (TCO) layers based on AZO was successfully demonstrated, but only achieved a PCE of 18%. Attempts to fabricate >100 cm² demonstrators were unsuccessful. Delays in achieving high-efficiency small-area devices and the time-intensive nature of full-wafer deposition and optimization prevented progress toward large-area proof-of-concepts.

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To advance vapour-processed perovskite/silicon tandem technology using thin industrial Cz wafers, future efforts should prioritize the reduction of electrical losses by diagnosing and optimizing series and shunt resistance pathways, particularly at the ITO/HTL interface and within textured-grown perovskite layers; the enhancement of photogeneration in thin silicon substrates through improved optical and texturing strategies; the development of scalable deposition tools capable of uniform, high-quality perovskite growth on large area to enable technology demonstration at industrially relevant formats.

These steps are essential to closing the gap between current performance and target efficiencies, and to validate the scalability of the approach

1.2. Relation with other activities in the project

The performance of tandem devices both in small and large area is related to most of the other work packages of the project, and in particular with WP3 and the development of high efficiency tandem modules.

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2. Results

2.1. Introduction, tandem expected values

At the start of NEXUS, the at that time record efficiency of perovskite/silicon tandem (PST) solar cells, using thick (>250 µm) float zone (FZ) monocrystalline silicon (c-Si) and solution-processed perovskite was 33.2 %[1], i.e. the target efficiency foreseen to be achieved at the end of the NEXUS project. This was achieved with the following parameters: an overall open-circuit voltage (V_{oc}) of approximately 1.96 V, short-circuit current densities (J_{sc}) close to 21 mA cm^{-2}, and fill factors (FF) exceeding 80%. To evaluate the feasibility of achieving these values with the devices developed in the framework of the project, it is instructive to first consider the performance of the single-junction (SJ) components.

NEXUS aimed to develop high efficiency PST devices with a particular focus on sustainability. In other words, the project aimed at demonstrating that the technology can be economically viable, environmentally responsible and socially acceptable. This implies, for example, the use of materials and processes that are compatible with industrial-scale production, the reduction of critical or scarce material consumption, and the reduction of greenhouse gases (GHG) emissions. High efficiency PST solar cells still mostly rely on the use of thick FZ c-Si wafers. In the literature, the use of Czochralski (Cz) wafers in PST solar cells is still rarely mentioned, although the number of examples has been increasing in recent years.[2] Yet the photovoltaic industry relies on Cz wafers due to the prohibitive cost of FZ wafers. The Life Cycle Costing (LCC) (deliverable D5.1) and environmental Life Cycle Analysis (e-LCA) (internal deliverable D5.3) carried out in the project have shown that the Si wafer remains the component that has the highest share of costs and is the highest source of GHG emissions, at the cell level. The social LCA (internal deliverable D5.4) also revealed that it is a major contributor to most of the studied indicators. In order for the economic, environmental, and social assessment of PST technology carried out in these reports to be relevant, the case studies used Cz c-Si wafers. Indeed, Cz wafers, as used by the PV industry, are not only much cheaper than the FZ wafers, but they are also much thinner (<150 µm), thereby directly reducing the impact of the Si wafer on material consumption and GHG emissions (as well as on most other indicators) per unit area. Consequently, if Cz Si already has the most significant negative impact on the majority of the technology's sustainability indicators, as revealed by the aforementioned reports, a sustainable PST technology can rely even less on FZ Si. The replacement of FZ Si with Cz Si is therefore the first and most important step towards the sustainability of the technology.

This is why the NEXUS consortium decided to work exclusively on Cz Si wafers, from the outset of the project. This choice comes with its challenges. Naturally, the Cz crystallization process introduces more impurities to the Si material than the FZ process does, thereby reducing the lifetime of photogenerated carriers compared to FZ silicon. However, this is not the most significant challenge, given that the current quality of Cz silicon does enable high efficiencies to be achieved [1], [2]. On the other hand, another challenge implied by this choice is the considerably lower thickness of industrial Cz wafers, which has, understandably, a significant impact on the capacity of the wafer to absorb light, particularly in the near infrared (NIR) range. This consideration is all the more important in the case of a PST cell, where photogeneration in the silicon cell depends exclusively on the absorption of NIR photons. In Figure 1, we have simulated the external quantum efficiency (EQE) of different PST solar cells made

[1] https://www.nrel.gov/pv/interactive-cell-efficiency

[2] For example, searching Scopus, with the query “TITLE-ABS-KEY (perovskite AND (silicon OR si) AND tandem) AND TITLE-ABS-KEY (czochralski OR cz)” returns only 19 results.

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with silicon heterojunction (SHJ) bottom cells based on double-side-textured Si wafers of different thicknesses. These optical simulations were carried out using the CROWM software, with the structure depicted in Figure 1 (left). The perovskite thickness was adjusted to 570 nm to ensure current matching with a 140-µm-thick bottom cell. The rear TCO was in this case a 70 nm tin-doped indium oxide (ITO) layer. The black solid curve in Figure 1 (right) is representative of the spectral response that would be obtained from a wafer with a thickness similar to that of typically used FZ wafers in PST devices (250 µm). Changing the wafer thickness to a value more representative of a Cz wafer from the PV industry (140 µm, red curve) results in a significant reduction in light absorption by the Si in the NIR, accounting for a reduction of 0.7 mA/cm² in the calculated bottom cell J_{sc}.

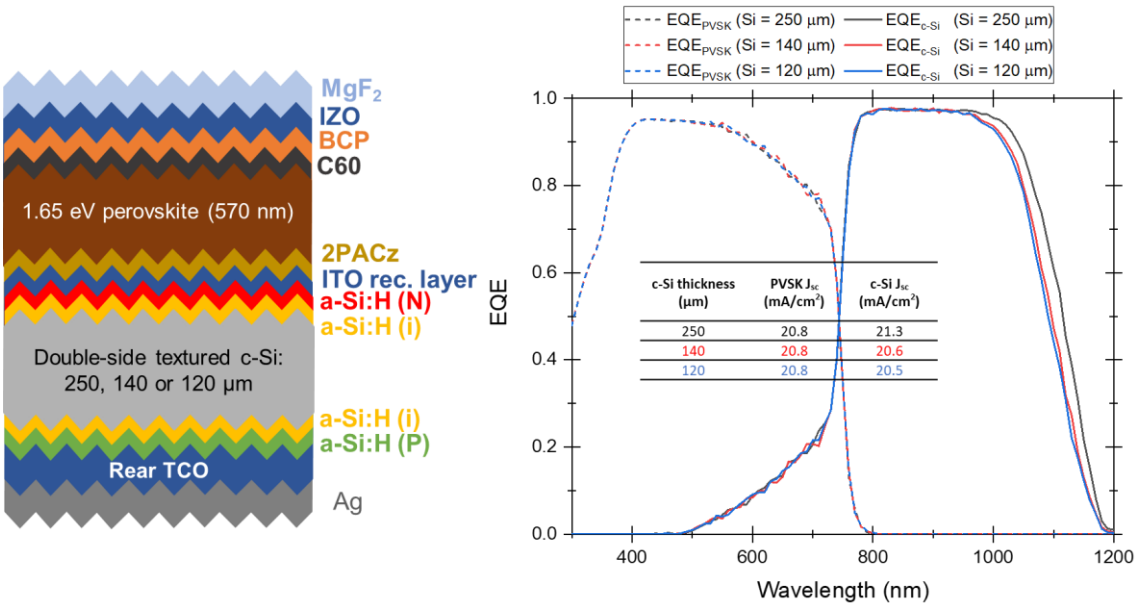

Figure 1: Simulated external quantum efficiency (EQE) of PST solar cells with Si bottom cells based on wafers of different thicknesses: simulated structure (left), share of photons absorbed by wavelength in the perovskite absorber (dashed lines) and in the c-Si wafer (solid lines) for three wafer thicknesses (250 µm (black), 140 µm (red) and 120 µm (blue)) (right). The inset table shows the short-circuit current of each sub-cell calculated from the EQE with the AM1.5 spectrum.

Another difficulty posed by the decision of building PST solar cells on Cz wafers is the surface morphology of diamond-wire-sawn Cz wafers that are purchased "as cut", i.e., with a very rough and defective surface covered with saw marks. In a typical Si-based solar cell manufacturing process, the defect-rich first micrometers close to the surface are etched in potassium hydroxide (KOH) in a so-called saw-damage removal step. In a second etching step, known as texturing, KOH is used in combination with a surfactant to control the anisotropic etching of the Si crystalline planes, leaving the surface covered with random-sized pyramids, typically in the µm range, thereby reducing wafer's surface reflection. In a monolithic PST solar cell, the perovskite is grown on top of the silicon bottom cell. This is why particular attention must be paid to controlling this complex surface morphology in order to make it suitable for this application. To this end, CEA initially concentrated its efforts on reducing the size of the pyramids to sub-micron scale using now commercially available surfactants designed to form smaller pyramids. However, the "nanotextured" surface obtained in this way still featured some isolated, larger pyramids, several µm in height, which could affect the continuity of the perovskite layer, thereby causing "shunt paths" in the top cell. These larger pyramids appeared to be the result of the saw-damage removal process that precedes texturing. This is why, in a second stage, we focused on improving the saw-damage removal step, in order to obtain the smoothest possible surface before performing the texturing. However, the optimization of the saw-damage removal

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process resulted in additional etching of Si material, causing the wafer thickness to be even further reduced. The wafers featuring the optimized saw-damage removal step with nanotexturing had indeed a thickness of about 120 µm, further reducing the Si bottom cell response in the infrared, as evidenced by the blue curve and further reduced J_{sc} Figure 1 (right).

In the literature, most PST devices manufactured with Cz Si-based bottom cells yield a Jsc of approximately 20 mA/cm² on 150 µm thick wafers, with the caveat that it is generally not specified whether this thickness is the "as cut" thickness or the effective thickness after etching [3], [4], [5], [6]. Results on thinner wafers (≤ 120 µm, effective "etched" thickness) are even less common in the literature, with reported J_{sc} of approximately 18 mA/cm² [7], [8], [9]. Most of the PST devices fabricated in the framework of NEXUS used SHJ bottom cells from CEA's pilot line. The M2-size (244 cm²) SJ SHJ cells manufactured in CEA's pilot line from 150-µm-thick wafers (effective thickness) with standard µm-scale texturing achieve efficiencies of 22.5% in average, with JV parameters of V_{oc} = 0.736 V, J_{sc} = 38.2 mA/cm², and FF = 0.80 when illuminated under 1 sun conditions [10]. This performance already indicates a limitation in the maximum current density achievable in the tandem configuration, as a rough estimation of the bottom-cell short-circuit current is typically taken as half the SJ value, yielding approximately 19 mA/cm² in this case, peaking at 19.5-19.8 mA/cm² when subtracting the shading from the metal grid used on M2 devices. As the V_{oc} also depends on the photogeneration, hence, when used in a tandem where half of the sun intensity is absorbed by the top perovskite cell, the remaining 0.5 sun that is absorbed in the Si cell reduces the V_{oc} to 0.7 V.

A slight reduction in performance is also expected when these wafers are cut into smaller pieces (typically between 2.5 × 2.5 cm² and 3 × 3 cm) to be used as bottom cells in tandem devices. This cutting process introduces minor losses in the initial JV parameters of the M2 cells (Figure 2, left). Moreover, subsequent depositions required to form the charge recombination junction and transport layers prior to the perovskite deposition can further decrease device performance. Figure 2 (Right hand panel) presents a study of the implied V_{oc} on 3 × 3 cm² silicon substrates, measured using the Sinton technique [11], illustrating that the co-evaporated layers induce only a small impact on the maximum achievable open-circuit voltage., illustrating that the processing of all the subsequent layers in the recombination layer and perovskite top cell (apart from the perovskite absorber) induce only a small impact on the maximum achievable open-circuit voltage.

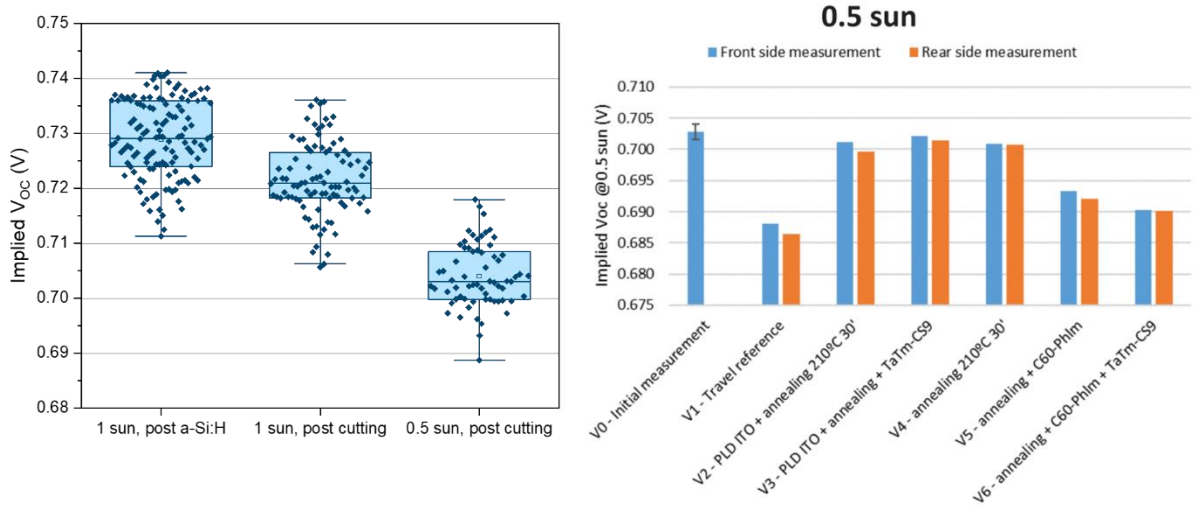

Figure 2: Implied V_{oc} measured by Sinton technique: at 1 sun on M2 wafers after a-Si:H deposition and at 1 sun and 0.5 sun after cutting them to 3x3 cm² substrates (left); at 0.5 sun on 3x3 cm² silicon substrates after different process steps of the PVSK top cell fabrication (right), V0 corresponding to the "0.5 sun, post cutting" measurement of the left graph. For this particular substrate, a maximum V_{oc} of the bottom cell is expected to

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be around 0.69 V.

Hence, from this analysis, for the small substrate sizes on the Cz wafers we find values of 19 mA/cm^2 and 0.69 V for Jsc and Voc, respectively. Assuming that the FF remains the same as on the M2 wafer (80%) the maximum power generated by the Si bottom cell is 10.48 mW/cm^2.

Figure 3 shows the JV curves and main photovoltaic parameters of the highest-efficiency opaque single-junction (SJ) perovskite top cells with a bandgap around ~1.68 eV fabricated using each deposition method presented in D1.2.

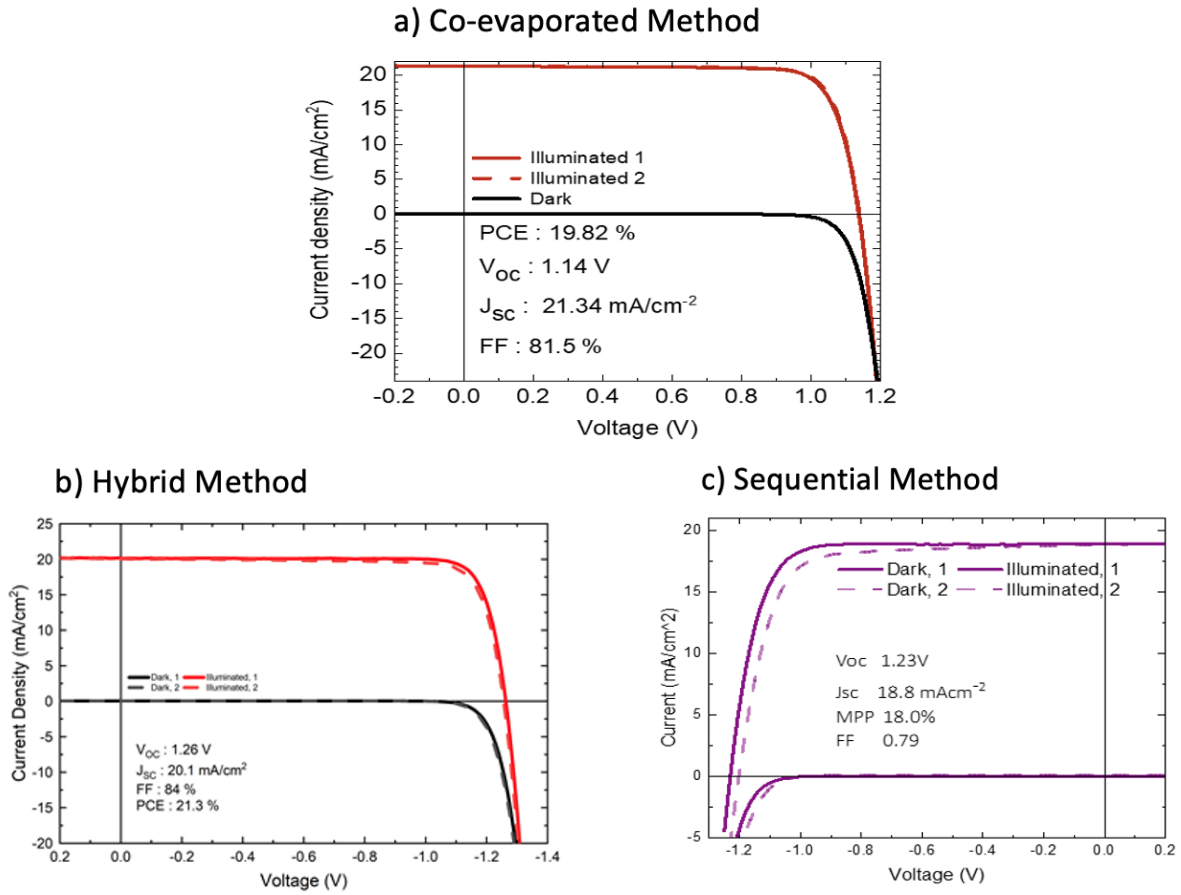

Figure 3: Best single junction top perovskite cells for the three different deposition methods.

The fully vacuum co-evaporated top cell achieved a power conversion efficiency (PCE) of 19.82%, with V_{oc} = 1.14 V, J_{sc} = 21.34 mA cm^{-2}, and FF = 81.5%. Using the hybrid method, where the inorganic elements of the perovskite are co-evaporated in a first step followed by the deposition of a solution containing the organic compounds, a PCE of 21.3% was obtained, corresponding to V_{oc} = 1.24 V, J_{sc} = 20.1 mA cm^{-2}, and FF = 84%. Finally, the sequential evaporation method (where the inorganics and organics are evaporated in two subsequent steps) yielded a PCE of 18.03%, with V_{oc} = 1.23 V, J_{sc} = 18.8 mA cm^{-2}, and FF = 78.0%.

Considering these values for the SJ cells, it is possible to estimate the maximum achievable values in the two-terminal (2T) tandem cell configuration. This is, for simplicity, done by summing the V_{oc} values and taking the limiting J_{sc} and FF. It should be noted that these devices are illuminated through the bottom (glass) side, while in a tandem configuration illumination takes place from the semitransparent

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top side. Thus, these estimations assume *ideal optical and electrical integration* within the tandem stack and, hence, indicate expected limitations in reaching the desired target of 33% efficiency. They are depicted in Table 1 below:

Table 1: Expected JV parameters of PST devices based on the JV parameters measured on the SJ cells composing the final tandem device.

	Si (0.5 sun)		Co-evaporated	Sequential evaporation	Hybrid	*Target KPIs*
Voc (V)	0.69	Voc sum	1.83	1.92	1.93	*2*
Jsc (mA cm^{-2})	19		21.34	18.8	20.1	*20.5*
FF (%)	80		81.5	78	84	*80.5*
Tandem PCE (%)			27.8	28.2	29.3	*33*

2.2. Champion tandem devices on small area

Surprisingly, when considering the SJ cell efficiencies, the highest efficiency achieved for small-area (1 cm^2) tandem devices was obtained using the sequential evaporation deposition method, reaching a power conversion efficiency (PCE) of 27.45%, only 0.75 point below our estimated efficiency assuming ideal integration in Table 1. The detailed photovoltaic parameters are V_{oc} = 1.93 V, J_{sc} = 19.7 mA cm^{-2}, and FF = 0.72. These results indicate that both the V_{oc} and J_{sc} exceed the expected values displayed in Table 1, while the FF remains below target. The low FF could be due to a number of reasons, the presence of shunt paths due to growth on the nanotextured silicon (as opposed to flat ITO coated glass in the SJ cells) and series resistance due to the nature of the ITO interlayer and subsequent evaporated hole transport layer (HTL) being unoptimized, as compared to the commercially purchased ITO glass/HTL interface. Figure 4 shows the corresponding JV curve and statistical distribution of the results (left), statistics of the measurements (center) and a scheme of the device (right).

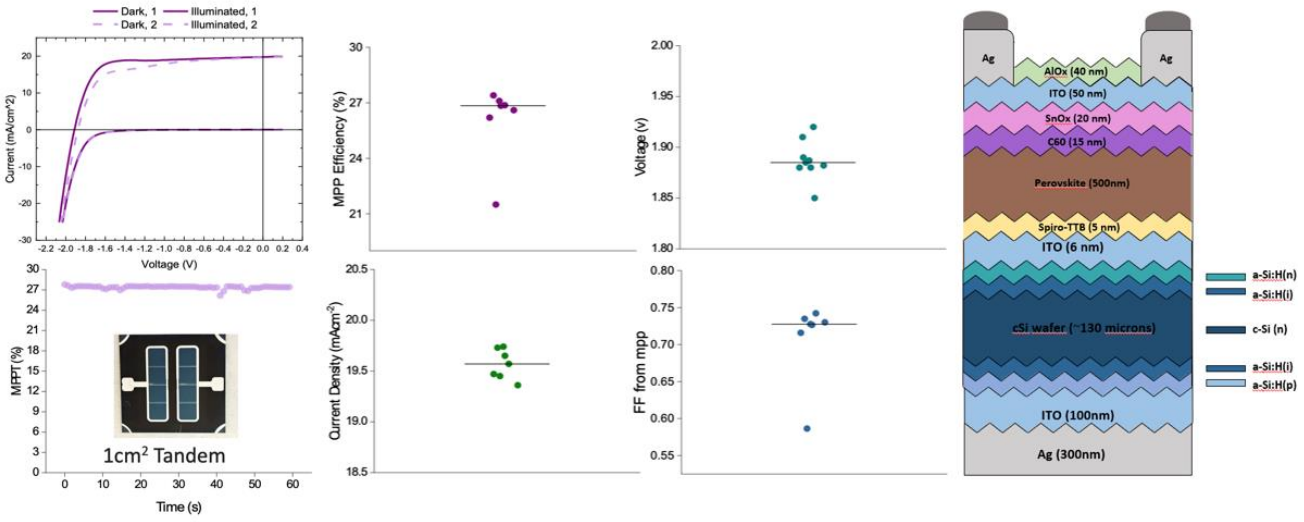

Figure 4: Highest efficiency device for small area reaching 27.45% PCE by sequential method of perovskite deposition.

PSTs incorporating co-evaporated perovskite top cells yielded a PCE of 27.2% (using a solution-processed self-assembled monolayer (SAM) as hole transport layer) on 1 cm² devices. The

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corresponding parameters were V_{oc} = 1.87 V, J_{sc} = 19.0 mA cm^{-2}, and FF = 0.73. Assuming the silicon bottom cell provides a V_{oc} ≈ 0.69 V, the top cell contributes approximately 1.18 V, which is slightly higher than the 1.14 V observed for single-junction devices. The JV characteristics for these devices are shown in Figure 5.

Finally, using the hybrid deposition method, a champion PST device with 27.02% PCE was demonstrated, with V_{oc} = 1.86 V, J_{sc} = 19.74 mA cm^{-2}, and FF = 0.73 (Figure 6). In this case, the V_{oc} lies 70/80 mV below the expected value in Table 1. The J_{sc} is as high as can be expected from the SHJ bottom cell. Once again, the FF remains below expectations, most probably due to subtle changes in the perovskite growth and in this instance solution conversion on textured silicon as opposed to flat ITO coated glass. Notably, although it is not implicitly proven, when we have thin HTL layers, or HTL layers with some pinholes leading to contact between the perovskite absorber layer and the TCO, we often observe hysteresis in the JV curves. The hysteresis that we observe her in the JV curves for both the sequentially evaporated and hybrid processed PSTs, is consistent with there being some directly contact between the perovskite and the ITO in the recombination layer in our PSTs processed on the textured silicon.

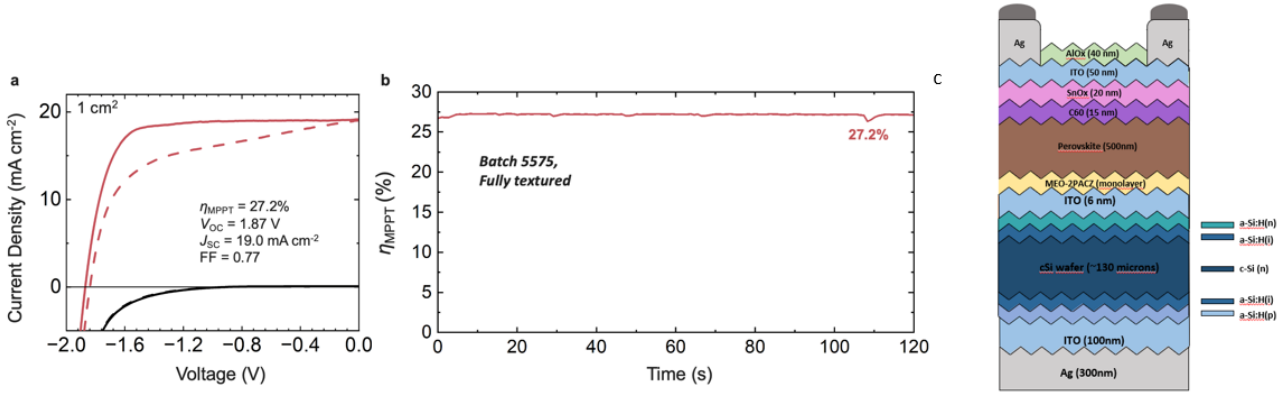

Figure 5: Tandem device with co-evaporated perovskite showing the highest efficiency for this type of deposition, PCE=27,2% (left, a). The high hysteresis may be due to contaminated SnO_2 layer. Maximum power point (MPP) tracking (center, b). Device stack (right, c)

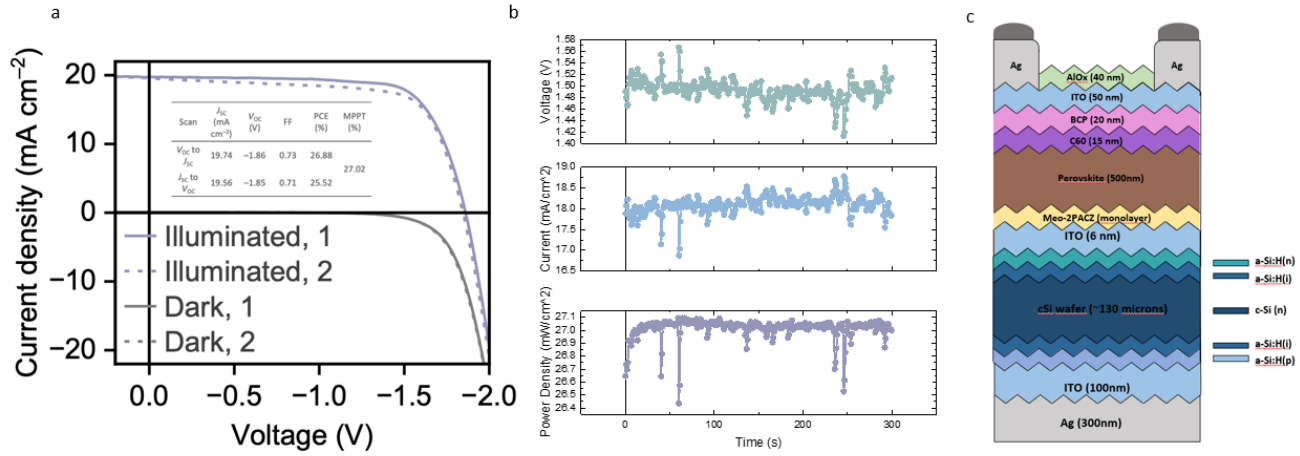

Figure 6: Tandem device with perovskite deposited following the hybrid method. It reached a maximum efficiency of 27.02% (left, a). Evolution of parameters for the first 5 minutes (center, b). Device stack (right, c).

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2.3. Large area tandem devices

2.3.1. Development of PST solar cells with an "intermediate" area layout

As stated in the project's first periodic report, it took approximately one year to obtain functional tandem devices with evaporated perovskites on Cz Si bottom cells in the project. This impacted other project activities that require solar cells, as well as the development of larger-area devices needed to demonstrate the feasibility of cell interconnection for a proof-of-concept module. As elaborated in the next section, the fabrication of full wafer or large area (> 100 cm^2) requires a huge amount of time, which is why an intermediate design was developed. As can be seen in Figure 7, the layout makes almost full use of the 3x3 cm^2 sample area thereby allowing the interconnection of several samples thanks to the larger active area and metal contacts, while maintaining the quantity of fabricated samples at a level similar to that of the 1 cm^2 active area devices. The active area of the layout, of 4.41 cm^2, provides first insights on the impact of upscaling when using vacuum-based and hybrid perovskite processes on (nano-)textured Cz wafers.

A larger-area device (4.41 cm²), fabricated using a similar sequential evaporation process for perovskite deposition as for the device shown in Figure 4, achieved a PCE of 26.8%. The slight reduction in performance compared to the smaller-area device primarily arises from a drop in V_{oc} to 1.83 V. Part of this will be due to averaging over a larger area, where we should compare with the average V_{oc} of ~ 1.88V for the 1cm^2 cells. The further differential of 0.05V may simply be down to batch-to-batch variation. On the other hand, the J_{sc}, at approximately 20 mA/cm^2, lies at the upper end of the range of devices fabricated in the project and the FF at a similar level to that of the 1 cm^2 devices. These results are presented in Figure 7.

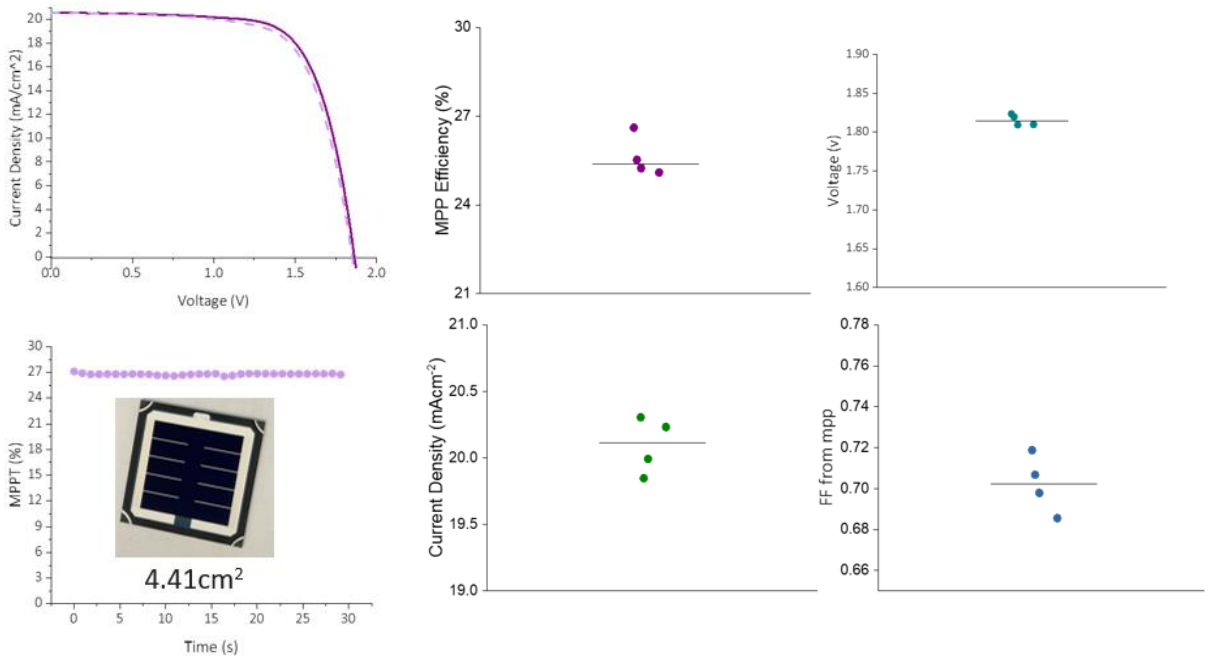

Figure 7: Champion device on 4.41cm2 area done with the sequential evaporation method. The PCE obtained with the champion device was 26.8%.

Larger-area devices (4.41 cm²) with hybrid-processed perovskite top cell were also fabricated; however, the champion device only reached only 21.5% PCE, mainly due to a significantly reduced fill

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factor (FF = 0.59), presumably due to inhomogeneities in processing uniformity over the entire substrate area.

2.3.2. Manufacturing attempts on 100 cm^2

Large area tandem devices with an active area of > 100 cm² have also been developed. They are based on a perovskite top cell deposited directly over an M2 silicon wafer. Among the three "top cell" partners of the consortium, only UOXF had the capacity, in terms of tool size, to carry out the fabrication of perovskite top cell layers on a full M2 wafer. As illustrated in Figure 8, the fabrication process involves sequential deposition of a rear ITO layer, followed by thermal evaporation of the back metal contact. The device stack is then completed with the evaporation of the hole transport layer (Spiro-TTB), the perovskite absorber, and the electron transport layers (C_{60} and SnO_2). Finally, an zinc-doped indium oxide (IZO) layer is applied as the transparent conductive oxide (TCO), and the device is shipped to CEA for final metallization and measurement. Notably, in the cluster deposition tool used at UOXF for the fabrication of the M2 tandem cell wafer, only one full-wafer cell can be fabricated each day. There were many failed attempts due to the need to adjust the automatic handling, which caused the wafers to break at various stages of the process. The handling system had only previously been used with thick metal holders for transporting small samples. Therefore, many adjustments were required to enable smoother handling and reduce the likelihood of wafer breakage. Finally, in the last weeks of the NEXUS project, we managed to deposit all layers in the PST stack at UOXF. The wafer cell back to CEA for front metallisation by screen printing and testing. Unfortunately, the wafer broke during shipping, despite the care taken over the packaging. We suspect that it was also weakened by the above-mentioned handling steps, as it already featured minor breakage at the corners which may have propagated throughout the entire wafer, due to additional mechanical stress (vibrations or brutal handling during transport, changes in pressure in the vacuum-sealed box used for the shipment).
Therefore, we were not able to obtain a result on a large-area device. This clearly indicates the need for suitable equipment for perovskite deposition on a large area in order to develop and fabricate devices on full wafers. A tool that allows deposition on just one wafer is insufficient, as processing one wafer at a time (one per day in our case, when everything goes well) takes too much time to allow for complete process optimisation, statistics generation, etc…

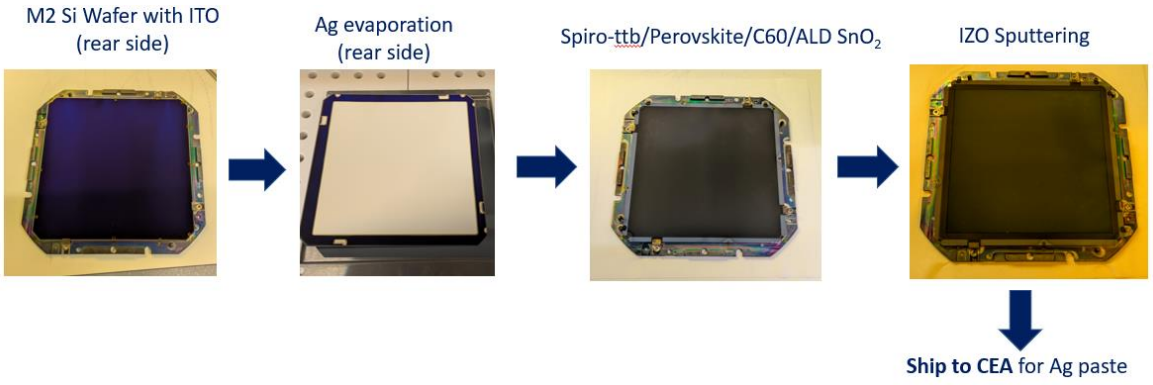

Figure 8: Process line for making 100cm² tandem device on M2 wafer size in UOXF's perovskite cluster.

2.4. Taking eco-design one step further with Indium-free TCO layers

The cells presented above represent enhanced sustainability design with reduced indium content with very thin ITO interlayers and thin ITO rear contacts, in addition to being based on Cz wafers. However, to further enhance the eco-design of the solar cells developed in NEXUS, we have evaluated the feasibility of partially or completely eliminating indium from these devices. Notably, at the time of writing the project proposal, indium was still included in the European Commission's list of critical raw materials[3]. It was however removed from the most recent version, published in 2023. Despite this recent reconsideration, the fact remains that indium is a scarce element and that its global production could be a limiting factor in the TW-scale era of photovoltaics [12].

In PST solar cells, indium is primarily present in the transparent conductive oxide (TCO) layers at both the rear and front of the tandem devices, which are typically made of doped indium oxide layers several tens of nm thick. A thin (< 10 nm) doped indium oxide layer is also typically used as charge recombination junction (CRJ) at the interface between the two sub-cells of the tandem device. In suppression was first developed and implemented for the rear TCO of the SHJ bottom cell, at SJ level, as described in internal deliverable D2.5 (In-free and enhanced sustainability Si bottom solar cell demonstrator). To this end, an aluminum-doped zinc oxide (AZO) layer was developed by magnetron sputtering. Similar V_{oc} and FF levels as with the ITO reference were obtained. However, the AZO layer absorbs more IR light than the ITO layer, as can be seen in Figure 9. Although we are considering the rear TCO, this stronger infrared absorption could affect the amount of light reflected at the interface with the metal electrode, which would impact the total amount of light ultimately absorbed by the bottom cell, and thereby its J_{sc}. To evaluate this impact, we performed optical simulations with CROWM, with the same stack as described in Figure 1, this time varying the rear TCO material, as well as the c-Si wafer thickness (Figure 9b). To perform the simulation, we used the refractive index and extinction coefficient of the ITO and AZO layers actually used in the fabricated PST solar cells, measured by ellipsometry. The simulated EQEs in Figure 9b show a significant reduction of the bottom cell response for the long wavelengths when using AZO as rear TCO. This leads to a reduction of 0.7 mA/cm^2 (resp. 0.9 mA/cm^2) in the 140-µm-thick (resp. 120- µm thick) bottom cell J_{sc} with respect to the cells using ITO as rear electrode. These simulation results show that a bottom cell combining a < 150 µm Cz wafer with an AZO-based rear electrode will probably strongly limit the current generated by the corresponding PST solar cell.

[3] https://rmis.jrc.ec.europa.eu/eu-critical-raw-materials

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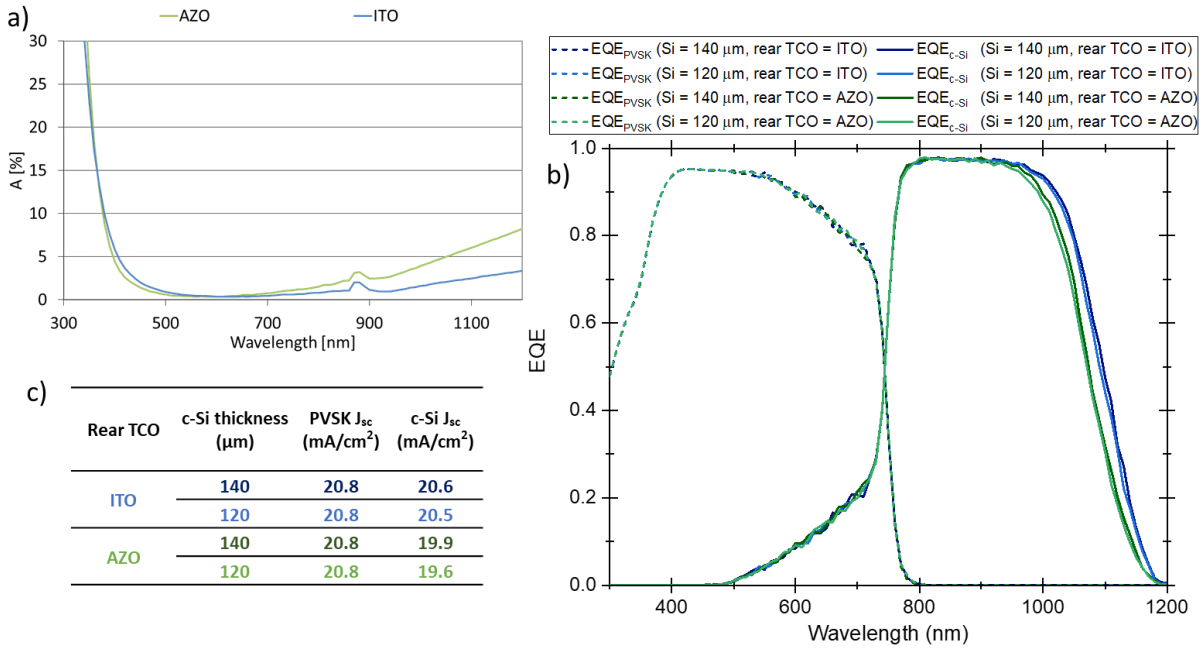

c)

Rear TCO	c-Si thickness (µm)	PVSK J_{sc} (mA/cm^2)	c-Si J_{sc} (mA/cm^2)
ITO	140	20.8	20.6
	120	20.8	20.5
AZO	140	20.8	19.9
	120	20.8	19.6

Figure 9: Replacement of rear ITO transparent electrode by AZO: Absorptance curves measure by spectrophotometry (a), simulated EQE of PST solar cells with either ITO (blue) or AZO (green) as rear TCO and bottom cells using either a 140 µm (darker colour) or 120 µm (lighter colour) wafer, c) J_{sc} values of each sub-cell for the different cases calculated from the EQE with the AM1.5 spectrum.

Nevertheless, to evaluate the impact of reducing In content in PST solar cells, UOXF fabricated tandem devices with the sequentially evaporated method on CEA bottom featuring an In-free rear TCO electrode and the thin (7nm thick) ITO recombination layer. To recall, the PST cells with ITO for both the front and rear electrodes exhibited, with an MPP efficiency of 26.8% over a 4.41 cm² aperture area, achieving a V_{oc} of 1.85 V, J_{sc} of 20.3 mA cm^{-2}, and a fill factor of 0.72. Substituting the rear ITO with AZO resulted in a marginal reduction in V_{oc} to 1.83 V and a more pronounced decrease in Jsc to 18.7 mA cm^{-2}, with a comparable fill factor of 0.72, yielding an overall MPP efficiency of 24.6%. We primarily attribute the reduced photocurrent to enhanced parasitic absorption within the AZO layer prior to reflection from the silver back contact. These findings highlight that indium-free rear electrodes can preserve the excellent voltage and fill factor characteristics of the tandem architecture, though further optical optimisation of the rear stack will be necessary to suppress absorption losses and fully recover photocurrent and hence efficiency. Notably, 4 of these cells with the AZO rear electrode were subsequently processed into modules, and put on outdoor testing in Ankara, which will be described in deliverable 4.6.

Moreover, pushing eco-design even further, an eco-friendly, completely In-free device architecture was developed. In this design, AZO was employed for both the CRJ and both front/rear TCO layers. Back TCO and CRJ were deposited at CEA by sputtering, while the front TCO was deposited at UVEG via pulsed laser deposition (PLD). A schematic comparison between the reference device and the eco-friendly design is shown in Figure 10, a).
The corresponding JV characteristics are presented in Figure 10, b). The eco-friendly tandem device achieved a PCE of 18%, slightly higher than that of the reference device which incorporated ITO at all contacts (16.9% PCE) in this batch. In both cases, the relatively low fill factors were attributed to high series resistances.

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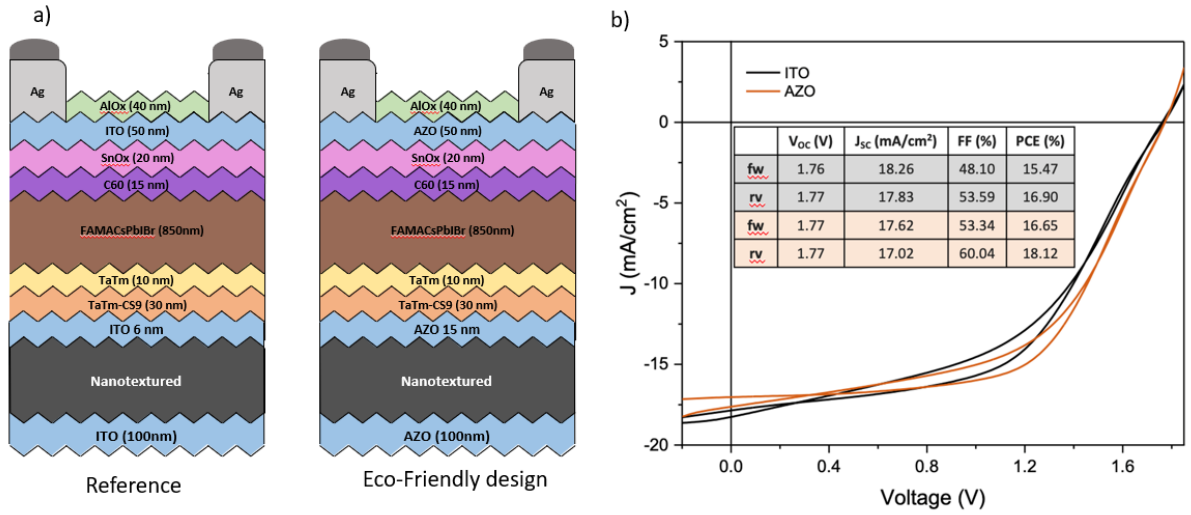
This work represents a proof-of-concept demonstration of an indium-free, sustainable tandem architecture and remains a work in progress aimed at optimizing both electrical performance and large-scale manufacturability.



	V_{OC} (V)	J_{SC} (mA/cm²)	FF (%)	PCE (%)
fw	1.76	18.26	48.10	15.47
rv	1.77	17.83	53.59	16.90
fw	1.77	17.62	53.34	16.65
rv	1.77	17.02	60.04	18.12

Figure 10: a) Standard tandem architecture using ITO as both TCO and CRJ (left, reference) and Indium free eco-design device (right) using AZO as replacement. b) JV characteristics of reference (black) and eco-friendly design (orange). In-free device achieved 18.1% PCE while in this case, the reference reached only 16.9% PCE.

3. Discussion: NEXUS results in relation to existing literature on PST solar cells

To date, only a handful of studies have demonstrated vacuum-processed perovskite/Si tandem solar cells, underlining how nascent this field remains compared to the well-established solution-processing routes. The earliest example by 9 et al. (2021) employed co-evaporation of a 1.53 eV perovskite absorber, achieving 24.7% efficiency (24.3% stabilized) with an operational stability over 1000 h under 1 Sun in N_2 atmosphere [13]. More recently, Xu et al. (2023) reached the current record efficiency of 27.4% using a 1.67 eV co-evaporated absorber with an open-circuit voltage (V_{OC}) of 1.82 V on a 0.25 cm² device [14]. Recent work from one of the NEXUS partners (UVEG) by Chozas-Barrientos et al. (2025) further explored co-evaporation combined with a molecular recombination junction, yielding 22.2% efficiency [15]. Alternative vacuum deposition routes have emerged only very recently: Zhang et al. (2025) reported low-pressure chemical vapor deposition (LPCVD) devices with 26.9% efficiency [16], while Mahboubi Soufiani et al. (2025) demonstrated sequentially evaporated top cells achieving 24.5% (24.0% stabilized) [17]. Despite these promising efficiencies, the total number of reports on vapor-based tandems – only five publications to date – remains negligible compared to hundreds for solution-processed tandems. Moreover, all the reported vacuum-based tandems remain limited to small areas (≤ 1 cm²), underscoring the urgent need for further process development and scalability studies to unlock their industrial potential. As shown in Figure 11 when compared against >100 solution-processed, ~20 hybrid-processed, and ~30 unspecified literature results, the NEXUS devices define a new performance frontier for vapor-processed tandems. The results achieved within NEXUS therefore represent a major breakthrough – 27.45%/26.8% for sequential evaporation (1/4.41 cm²),

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27.2% for co-evaporation (1 cm²), 27.05 % for the hybrid approach (1 cm²) – demonstrating, for the first time, that fully vacuum-based processes can consistently deliver efficiencies competitive with the hybrid approach (in our case on the same type of bottom cell) while being inherently more scalable and industrially compatible. While the ultimate project target of >33% (1 cm²) remains aspirational, having been achieved just by a handful of research groups worldwide with solution processed perovskites (see Figure 11), our results represent a step-change in maturity and device area for these deposition techniques. These advances confirm that the underlying vacuum routes are approaching the performance threshold required for industrial transfer, bridging the gap between laboratory demonstration and scalable, high-throughput manufacturing. This is even more meaningful given that these results were obtained on industry-relevant silicon substrates, making them almost unique.

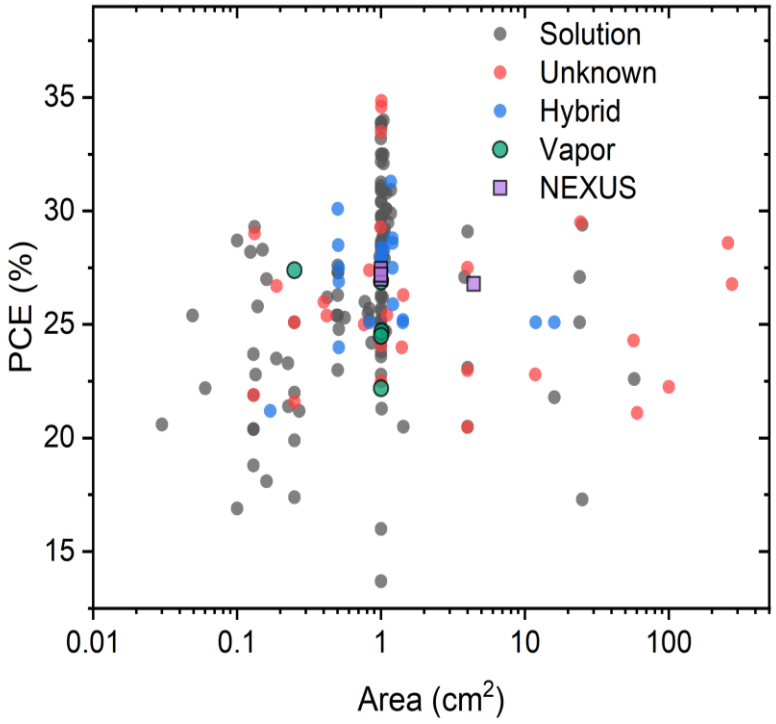

Figure 11: Highest reported PCEs of perovskite/Si tandem solar cells for different deposition techniques plotted over area. The highest PCEs achieved within NEXUS (hybrid + vapor) are also shown.

While these results are relevant and commendable, they also demonstrate that significant improvements are needed to bridge the gap between the project's targets and the efficiencies of world-record devices.

On the Si bottom cell side, one strong drawback with respect to the values needed to achieve the efficiency target was the available photogenerated current. This was imputable to the choice of working on Cz wafers from the PV industry, that are significantly thinner than the thick FZ wafers typically used to make champion PST devices. This means that the continuous reduction in thickness of commercial Cz wafers [18] clearly poses a challenge in terms of counterbalancing the current generated by the perovskite top cell. In the framework of NEXUS, the thinnest wafers used to make tandem devices were approximately 120 µm thick, after a particularly harsh etching process of 170-µm-thick as-cut wafers to optimize their surface morphology. Nowadays, 120 µm is the thickness of as-cut wafers available for purchase from Si suppliers. In the future, optimization of the wet chemical treatment of the Si surface to reduce material etching, enhanced light-management of the Si bottom

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cell or adjustment of the perovskite composition will be necessary to compensate for the loss of photogeneration in the silicon associated with the reduction in thickness.
On the perovskite top cell side, the SJ devices fell short in terms of V_{oc} with respect to the project's target KPI of 1.3V, one reason being the difficulty to find satisfying passivation strategies for vacuum-processed perovskite, as already pointed out in deliverables 1.1 and 1.3.
When it comes to tandem integration, a particularly low FF is obtained, due to both non-optimal series and parallel resistances. A probable reason for the too high series resistance is a non-optimal interface between the TCO CRJ and the top cell HTL, which is the exact interface, where the two independently-optimized sub-cells are in contact. Future developments should focus on understanding and optimising this interface to unlock higher efficiencies.

4. Conclusion

The targeted efficiencies of 33% for small area cells and 30% efficiency for 100cm^2 cells have not been reached due to underperforming sub-cells and more significant than anticipated challenges with scaling up to full-wafer scale handling and deposition. The best PST devices made in NEXUS achieved MPP-tracked PCEs of 27.45%/26.8% (1/4.41 cm²) with a sequentially-evaporated perovskite top cell, 27.2% (1 cm²) with a co-evaporated top cell and 27.05% (1 cm²) with hybrid-processed top cell. All were fabricated on industrially processed SHJ bottom cells using Cz wafers from the PV industry. While falling short of the efficiency objectives, the results, obtained with the combination of a fully vacuum-processed perovskite and a thin Cz Si bottom cell, are almost unique in the literature and demonstrate the potential of an unscalable technique for perovskite deposition on substrates that are representative on the Si PV industry.

The underperformance of the Si subcell is noted primarily in the J_{sc} and a little bit in the V_{oc}. For example, if the Si cell would produce 21 mA/cm^2 under 0.5 sun (as in the record cell stated in the introduction), and assuming the measured V_{oc} and FF of the SHJ cell, the addition of the sequentially evaporated perovskite would lead to a tandem efficiency of 31.4% (keeping the V_{oc} of the Si cell at 0.69 V, 1.23 V for the perovskite cell, and the limiting junction FF of 0.78). The limited J_{sc} of the industrial Cz wafers is due to their limited as-purchased thickness (compared to the thick FZ wafers typically used in PST literature), combined with the different etching steps used to obtain an optimized surface morphology, resulting in a substrate thickness < 120 µm.
The performance of the perovskite subcell slightly falls short of expectations in terms of V_{oc}. The project's target KPI was 1.3 V, which would have enabled higher efficiency in the tandem cells to be achieved.
The integration of the perovskite cell on the textured Si bottom cell is obtained with virtually no losses in V_{oc}. The obtained V_{oc} of the tandem cells is very close to the sum of the individual V_{oc}'s. However, the FF in the tandem cells is consistently lower than that of either sub-cell. In actuality, the FF of the tandem cell should be higher than that of either sub-cell due to the comparably lower J_{sc} and higher V_{oc} values. Hence, electric losses in our PSTs are significant, due to both high series resistance, possibly resulting from a non-optimal ITO CRJ/HTL interface, and reduced shunt resistance, probably caused by shunt paths in the perovskite in relation to its growth on a textured substrate.

Reduced-indium cells, with a rear AZO transparent electrode, have also been demonstrated, yielding to slightly reduced performance, with a 24.6% MPP-tracked PCE, compared to their counterparts with rear ITO. The J_{sc} is even lower in the reduced-In devices, which we attribute to increased parasitic absorption at the rear of the Si bottom cell. As a proof of concept, completely In-free cells were also

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demonstrated. In the precise fabrication run, they achieved comparable efficiencies to the In containing reference cells, however, the efficiency of both cell types was < 19%. This is promising, however more effort is needed to verify the validity of the entirely In-free approach, particularly with regard to the CRJ.

The attempts to make a large-area (> 100 cm^2) demonstrator unfortunately did not work out. This was due to the overall delay in reaching high efficiency PST devices in the project, combined with the highly time-consuming process needed to fabricate and optimize devices on full wafer scale.

In summary, to further improve the efficiency of PST devices made with vapour-processed perovskite top cells and thin Cz Si bottom cells, future work should focus on understanding the series and parallel resistance losses to achieve higher FF, and enhancing the photogeneration in the thin Si bottom cells. To demonstrate the technology's feasibility on a larger scale, suitable tools for large area deposition of the perovskite will be needed.

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